

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 1 and 9-11 as follows:

1. (Currently Amended) A delay element, comprising:

an input signal to be delayed; and

a series of at least two delay stages;

wherein each of the delay stages includes a stack of uniform ~~minimum~~ channel length transistors with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other circuits on a chip;

wherein the use of uniform ~~minimum~~ channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip;

wherein a gate of each of the transistors in each of the delay stages are electrically coupled together to form an input in each of the delay stages;

wherein a source of a top transistor in the stack is coupled to a first reference voltage;

wherein a source of a bottom transistor in the stack is coupled to a second reference voltage;

wherein a drain of the top transistor is electrically coupled to a drain of the bottom transistor in the stage so as to form an output of the stage;

wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and

wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.

2. (Previously Presented) The delay element according to claim 1, wherein each stack of transistors includes additional transistors electrically coupled with the top transistor and the bottom transistor;

wherein a drain of a first additional transistor is electrically coupled to a source of the top transistor, a drain of the last additional transistor is connected to a source of the bottom transistor; and

wherein a drain of each of zero or more remaining additional transistors is electrically coupled to a source of an adjacent transistor within the remaining additional transistors so as to form a totem pole configuration for the stack.

3. (Previously Presented) The delay element according to claim 1, wherein each transistor of the second conductivity type is a n-channel FET.

4. (Previously Presented) The delay element according to claim 1, wherein each transistor of the first conductivity type is a p-channel FET.

5. (Previously Presented) The delay element according to claim 2, wherein each transistor of the second conductivity type is a n-channel FET.

6. (Previously Presented) The delay element according to claim 2, wherein each transistor of the first conductivity type is a p-channel FET.

7. (Original) The delay element according to claim 1, wherein the input signal to be delayed is a clock signal.

8. (Previously Presented) The delay element according to claim 2, wherein the input signal to be delayed is a clock signal.

9. (Currently Amended) A memory circuit comprising:

at least one delay element; wherein the delay element includes:

an input signal to be delayed; and

a series of at least two delay stages;

wherein each of the delay stages includes a stack of uniform minimum channel length transistors with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other memory circuits on a chip;

wherein the use of uniform minimum channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other memory circuits;

wherein a gate of each of the transistors in each of the delay stages are electrically coupled together to form an input in each of the delay stages;

wherein a source of a top transistor in the stack is coupled to a first reference voltage;

wherein a source of a bottom transistor in the stack is coupled to a second reference voltage;

wherein a drain of the top transistor is electrically coupled to a drain of the bottom transistor in the stage so as to form an output of the stage;

wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and

wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.

10. (Currently Amended) A clock circuit comprising:

at least one delay element, wherein each delay element includes:

an input signal to be delayed; and

a series of at least two delay stages;

wherein each of the delay stages includes a stack of uniform ~~minimum~~ channel length transistors with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other clock circuits on a chip;

wherein the use of uniform ~~minimum~~ channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other clock circuits;

wherein a gate of each of the transistors in each of the delay stages are electrically coupled together to form an input in each of the delay stages;

wherein a source of a top transistor in the stack is coupled to a first reference voltage;

wherein a source of a bottom transistor in the stack is coupled to a second reference voltage;

wherein a drain of the top transistor is electrically coupled to a drain of the bottom transistor in the stage so as to form an output of the stage;

wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and

wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.

11. (Currently Amended) A delay circuit comprising at least one stack of transistors, each of the at least one stack of transistors comprising:

a first transistor with a source electrically coupled to a first reference voltage;

a last transistor with a source electrically coupled to a second reference voltage;

a totem pole of at least two transistors, the totem pole including:

a top transistor with a source electrically coupled to a drain of the first transistor;

a bottom transistor with a source electrically coupled to a drain of the last transistor; and

at least two transistors, wherein the transistors complete the totem pole arrangement, wherein a drain of each of the transistors is electrically coupled to a source of an adjacent transistor within the transistors relative to the each of the transistors, and wherein each of the transistors within the totem pole comprise a uniform minimum channel length transistor with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other delay circuits on a chip, the use of uniform minimum channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other delay circuits;

an input electrically coupled to each gate within the totem pole; and

an output electrically coupled to connection between one source and one drain of two transistors within the totem pole;

wherein when the input is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and

wherein when the input to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.

12. (Previously Presented) The delay circuit according to claim 11, wherein each transistor of the first conductivity type is a p-channel FET.

13. (Previously Presented) The delay circuit according to claim 11, wherein each transistor of the second conductivity type is a n-channel FET.

14. (Previously Presented) The delay circuit according to claim 11, wherein the input signal to be delayed is a clock signal.